WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

a trench selectively formed which extends from a surface of said semiconductor substrate to a predetermined depth;

an isolation insulating film buried in said trench, each of upper portions of said semiconductor substrate which are isolated from each other by said isolation insulating film being defined as a transistor region where a predetermined transistor of an insulated gate type is to be formed;

a first semiconductor layer formed along a side face of said trench in said transistor region; and

a second semiconductor layer formed in a portion of said first semiconductor layer which is close to said side face of said trench, wherein

said second semiconductor layer contains a predetermined impurity of the same conductivity type as a channel region of said predetermined transistor, and

said first semiconductor layer has a property of suppressing diffusion of said predetermined impurity which is caused by a heat treatment.

2. The semiconductor device according to claim 1, wherein

said first semiconductor layer includes an SiGe layer,

said predetermined impurity includes B (boron), and

said second semiconductor layer includes a B-containing SiGe layer which is an SiGe layer containing B.

3. The semiconductor device according to claim 1, wherein

said first semiconductor layer includes an SiGe layer,

said predetermined impurity includes In (indium), and

said second semiconductor layer includes an In-containing SiGe layer which is an SiGe layer containing In.

4. A method of manufacturing a semiconductor device comprising the steps of:

(a) selectively forming a trench extending from a surface of a semiconductor substrate to a predetermined depth;

(b) implanting a first impurity toward a side face of said trench in said semiconductor substrate, to form a first impurity implanted region along said side face of said trench in said semiconductor substrate;

(c) implanting a second impurity toward said side face of said trench in said semiconductor substrate, to form a second impurity implanted region within said first impurity implanted region;

(d) activating said first and second impurities in said first and second impurity implanted regions by carrying out a heat treatment after said steps (b) and (c), to form a first semiconductor layer and a second semiconductor layer along said side face of said trench in said semiconductor substrate;

(e) forming an isolation insulating film in said trench, each of upper portions of said semiconductor substrate which are isolated from each other by said isolation insulating film being defined as a transistor region where a predetermined transistor of an insulated gate type is to be formed; and

(f) forming said predetermined transistor in said transistor region, wherein

said second impurity includes an impurity of the same conductivity type as a channel region of said predetermined transistor, and

said first semiconductor layer has a property of suppressing diffusion of said second impurity.

5. A method of manufacturing a semiconductor device comprising the steps of:

(a) selectively forming a trench extending from a surface of a semiconductor substrate to a predetermined depth;

(b) implanting a first impurity toward a side face of said trench in said semiconductor substrate, to form a first impurity implanted region along said side face of said trench in said semiconductor substrate;

(c) activating said first impurity in said first impurity implanted region by carrying out a heat treatment after said step (b), to form a first semiconductor layer along said side face of said trench in said semiconductor substrate;

(d) implanting a second impurity toward said side face of said trench in said semiconductor substrate, to form a second impurity implanted region within said first semiconductor layer;

(e) activating said second impurity in said second impurity implanted region by carrying out another heat treatment after said step (d), to form a second semiconductor layer in said first semiconductor layer;

(f) forming an isolation insulating film in said trench, each of upper portions of said semiconductor substrate which are isolated from each other by said isolation insulating film being defined as a transistor region where a predetermined transistor of an insulated gate type is to be formed; and

(g) forming said predetermined transistor in said transistor region, wherein

said second impurity includes an impurity of the same conductivity type as a channel region of said predetermined transistor, and

said first semiconductor layer has a property of suppressing diffusion of said second impurity.

6. The method of manufacturing a semiconductor device according to claim 4, wherein

said semiconductor substrate includes a silicon substrate,

said first impurity includes Ge (germanium),

said second impurity includes B (boron),

said first semiconductor layer includes an SiGe layer, and

said second semiconductor layer includes a B-containing SiGe layer which is an SiGe layer containing B.

7. The method of manufacturing a semiconductor device according to claim 4, wherein

said semiconductor substrate includes a silicon substrate,

said first impurity includes Ge (germanium),

said second impurity includes In (indium),

said first semiconductor layer includes an SiGe layer, and

said second semiconductor layer includes an In-containing SiGe layer which is an SiGe layer containing In.

8. The method of manufacturing a semiconductor device according to claim 5,

wherein

said semiconductor substrate includes a silicon substrate,

said first impurity includes Ge (germanium),

said second impurity includes B (boron),

said first semiconductor layer includes an SiGe layer, and

said second semiconductor layer includes a B-containing SiGe layer which is an SiGe layer containing B.

9. The method of manufacturing a semiconductor device according to claim 5, wherein

said semiconductor substrate includes a silicon substrate,

said first impurity includes Ge (germanium),

said second impurity includes In (indium),

said first semiconductor layer includes an SiGe layer, and

said second semiconductor layer includes an In-containing SiGe layer which is an SiGe layer containing In.